6G-RIC
Research and
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GEFÖRDERT VOM
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2D Sampled-Beamforming Receiver with A-to-D Conversion

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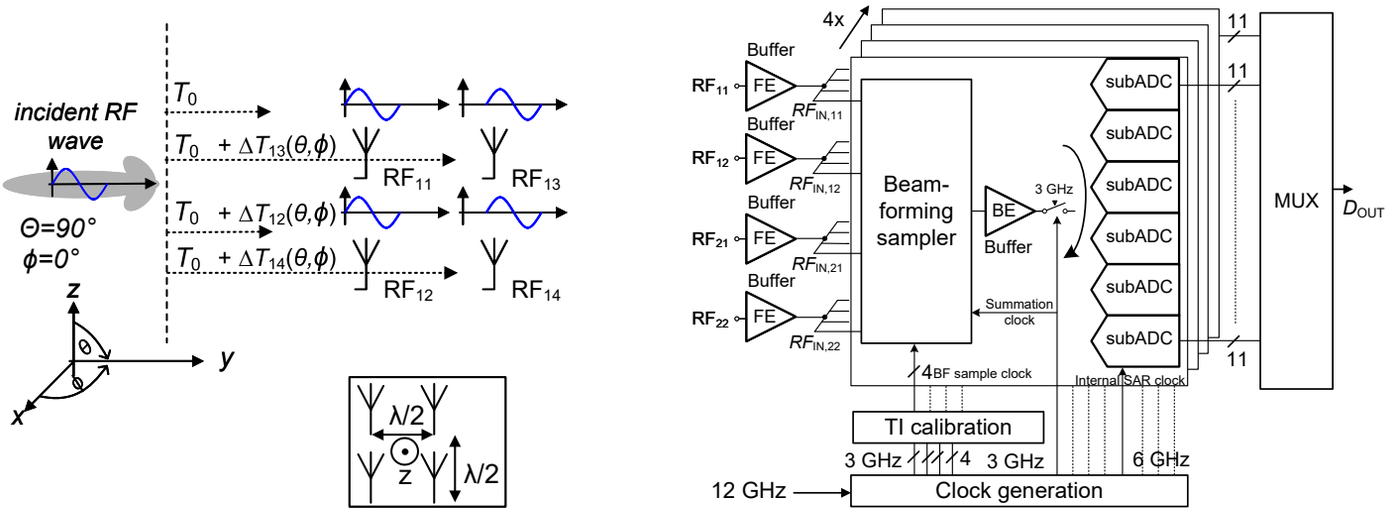
How to monolithically combine a 2D-NxM antenna-array in an energy-efficient manner with GHz of channel bandwidth? How to solve the channel spacing and combining problem with smallest silicon form factor? How to provide accurate delay/phase tuning across 2 dimensions?



The architecture study shown above shows a 2x2 beamforming receiver architecture. The RF inputs are isolated with push-pull source followers providing both high linearity and high bandwidth. The receiver study uses for the first time a sample-based beamforming architecture with a true time delay generated from a clock delay network with uniform 10ps time steps. As a result, all inputs are sampled in phase without any phase shifter in the RF path. Charge-based summation enables an ultra-low power beam-forming function that avoids any wavelength dependence. The final combined 6GHz bandwidth output signal is buffered prior to final A/D conversion, ensuring high linearity.

KEY FINDINGS

Future 6G wireless transceivers will require a large signal bandwidth to support high data rates. Due to higher carrier frequencies and transmit power losses, beamforming is key to overcoming path loss and improving spectral efficiency. This need is driving the development of a novel, compact, low-power, charge-based beamforming receiver that supports signal bandwidths beyond 6 GHz with the highest linearity and SNR performance. Initially, mathematical analysis and front-end design are conducted to explore the new sample-based beamforming approach. Key design aspects include beamforming gain, steering accuracy, front-end linearity, and noise performance. A 12GS/s 2D beamforming front-end with a 10ps delay step size for signal frequencies up to 6GHz has been developed to demonstrate the concept. Next, a beamforming receiver ADC using multiple SAR sub-ADCs is being developed to achieve a 12GS/s sampling rate, with SFDR exceeding 68dBc and SNR above 55dB. In summary, we have designed a complete RF-to-digital receiver system, combining a 2D antenna array, precise gain and phase tuning, and A-to-D conversion, providing multi-GHz channel bandwidth with optimal SNR and linearity.

E. Wittenhagen, F. Gerfers, "An 11-Bit 12 GS/s Beam-Forming Receiver ADC for a 2x2 Antenna Array utilizing True Time-Delay with 68 dBc SFDR and 55 dB SNDR," 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, Singapore, 2024, pp. 1-5.

E. Wittenhagen, P. Artz, P. Scholz, F. Gerfers, "A 3-GS/s RF Track-and-Hold Amplifier Utilizing Body-Biasing With >55-dBFS SNR and >67-dBc SFDR Up to 3 GHz in 22-nm CMOS SOI", 2022, IEEE Open Journal of the Solid-State Circuits Society, vol. 2, 2022.