6G-RIC
Research and
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GEFÖRDERT VOM
Bundesministerium
für Bildung
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D-Band Receiver Design based on 22nm CMOS Building Blocks

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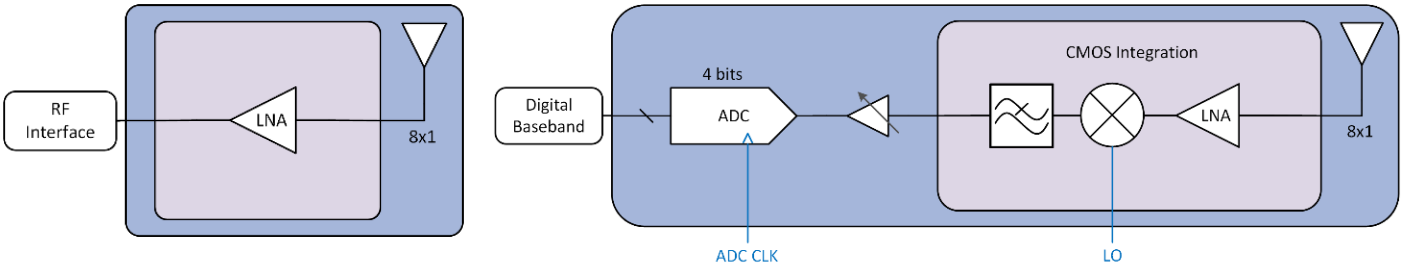
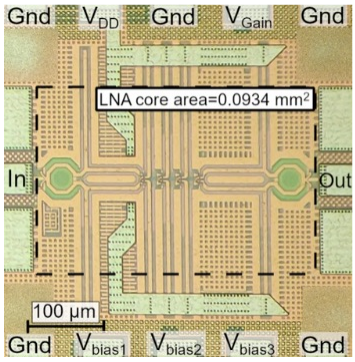
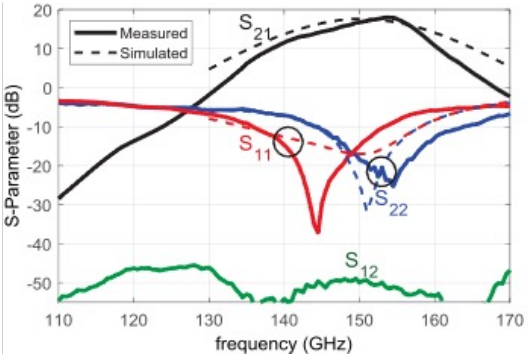
How can receivers be implemented in D-Band?







Proposed demonstrator design; Fig. 1. The first demonstrator consists of an 8x1 antenna array with an integrated LNA, the RF-interface will be realized using waveguides; Fig. 2. Final demonstrator, all circuit components integrated into one monolithic IC, LO and ADC CLK will be supplied externally. Fig. 3 Simulated and measured S-Parameters and die photograph of the LNA [1]

KEY FINDINGS

The first iteration of the proposed demonstrator will consist of an 8x1 antenna array, one LNA and a waveguide interface. A combiner will be used to obtain a single output from the array. This demonstrator will allow to test the performance of the antenna array. The CMOS LNA design features a 10GHz bandwidth centered around 150GHz (D-Band 110-170GHz), with an adjustable gain between 9.0 to 18.0dB. The power consumption scales accordingly from 17.5 to 27.5mW. As conventional planar antennas are not able to reliably achieve the design goals of the antenna array, a substrate-integrated waveguide topology using a common thin-film process will be used to construct the array. It is expected that a bandwidth of up to 20% and a single element gain of up to 8dBi can be achieved.
The second iteration of the demonstrator will feature a down-conversion mixer, accompanied by a low-pass filter and an ADC. All high-frequency circuit components will be integrated on monolithic IC using a 22nm CMOS FDSOI process.
First tests are expected to take place later this year in Q4 2024, with the second demonstrator expect to be ready later in 2025.

P. J. Artz, P. Scholz, T. Mausolf and F. Gerfers, "A Fully-Differential 146.6-157.4 GHz LNA Utilizing Back Gate Control to Adjust Gain in 22 nm FDSOI," 2022 IEEE/MTT-S International Microwave Symposium - IMS 2022, Denver, CO, USA, 2022, pp. 611-614